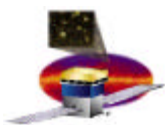


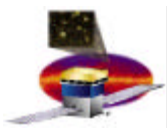
Electronics Design

James Ampe
NRL / Praxis, Inc.



Updated Status, Recent Changes

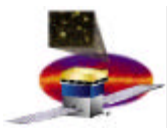
- ❑ Review of things that have changed for Cal Electronics:
 - AFEE board design and layout being done at SLAC. NRL has parts, testing and verification responsibility.
 - PIN diode to AFEE connection implemented by twisted-pair wires instead of flex cable.
 - GCRC chip package is going to larger body plastic package, 14x14 mm instead of 12x12 mm.



Updated Status, Flight Design

☐ Present Flight Design Status

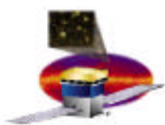
- Have been testing pre-pre EM X AFEE Board.
- Pre EM Y AFEE board is near end of layout at SLAC.
- Connector manufacturer being switched from Cristek to Microdot (formerly Nanonics) and Airborn. Will use some Cristek connectors for EM boards.
- Fuse selection and some ceramic capacitor selection is still being made.
- LVDS communication biasing currents are still to be chosen. Bias currents are set by resistors on the AFEE board.



Electronics Issues, AFEE

❑ AFEE Issues

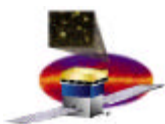
- AFEE Grounding method still to be decided
- AFEE Thermal design still to be verified, implemented and tested.
- AFEE circuit board design is still to be checked to IPC and NASA standards.
- AFEE circuit board design is still to be checked for bowing/warping considerations.
- AFEE LVDS communication reliability is yet to be finalized.
 - May be seeing some on-board interference in the LVDS signals with the present pre-pre X AFEE board. Needs more testing.
 - Pre EM Y board layout is different enough from present AFEE board to give different performance in this regard.



Electronic Issues, GCRC

❑ GCRC ASIC Issues

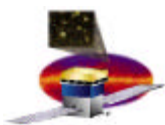
- Changing to different plastic package for the GCRC requires new test boards.
 - GCRC vector testboard is yet to be redesigned and manufactured.
 - Still have noisy trigger outputs of GCRC on test board.
 - » Have tried a few possible solutions without success, but still have a few remaining possible solutions.
 - » Need to have a board design with quiet triggers prior to redoing the test board.
- Working on modified VHDL code for a GCRC ver 5 ASIC submission
 - GCRC v4 will be used for EM calorimeter. Ver 5 could be used for flight.
 - Modifications in Ver 5 code:
 - 2 bit read/write code instead of 1 bit, as done for ACD and Tracker.
 - Implement Reset command, gives row addressable resets.
 - Digital filtering of reset line, less susceptible to line glitches.
 - Change trigger request to TEM as simple digital-sampled row trigger. Remove trigger de-glitching and inhibits.
 - Include hard wired readable GCRC version number.
 - » Gives confidence of which VHDL code is implemented.



Electronic Issues, GCFE

❑ GCFE ASIC Issues

- Have usable GCFEv7 for Cal EM.
- Ver 8 GCFE design to be submitted.
 - Modifications in Ver 8:
 - Gate out inadvertent triggers during preamp reset interval.
 - Have programmable register bit to turn off automatic preamp reset.
 - Increase output buffer gain to increase linear range from 2+ volts to 2.5 volts.
 - Modify charge injection capacitor values to be able to test autoranging function.
 - Give x8 sample and hold more of an offset to take care of some chips having a low offset, in the non-linear region.
- GCFEv7 Test results:
 - Linearity is good.
 - Noise is not too bad, on the order of the design goal of 2000 electrons.
 - Sampling stage appears to add noise.
 - There are some increased noise effects at lower temperatures.
 - PIN diode capacitance greatly reduces the problems.
 - Still investigating.



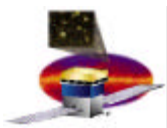
Electronic Issues, Connections

❑ PIN Diode Connections

- **PIN diode attachment changed from flex cable to twisted-pair wires.**
 - Mechanical design changes to implement this are complete.
 - Testing with mockup has not started.

❑ TEM – Cal Connections

- **Plan to change flight connector manufacturer from Cristek to Microdot and Airborn.**
 - Received shipment of 69 pin micro connector with mounting jackposts instead of jack screws.
 - Customer service on this problem was lousy.
 - Received shipment of 37 pin nano connectors with incorrect pinout.
 - Customer service on this from their quality assurance person was non-existent.
- **Will use a combination of connectors for the EM cal boards designated for software testing.**



Electronic Issues, Schedule

- ❑ **Schedule for assembled EM AFEE boards is slipping.**
 - **First draft completion of AFEE board layouts by SLAC have slipped.**
 - **Time between first draft and acceptance of AFEE board layout will cause more slip.**
 - **Do not have all EM board parts in hand.**